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DESIGN OF LOW POWER REVERSIBLE MULTIPLIER

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ABSTRACT

Reversible computing is a promising alternative to these technologies, with applications in ultra-low power, nano computing, quantum computing, low power CMOS design, optical information processing, bioinformatics etc. In reversible logic the power dissipation can be minimized or even eliminated. Power dissipation is one of the most important factor in the VLSI circuits design .In this paper a 4x4 reversible multiplier circuit is proposed with the design of two new reversible gates called ABC and GPS gates. In this paper the reversible multiplier circuit is designed by using GDI low power technique and is compared with conventional CMOS in terms of area and power. And this done by using Tannar tools.

KEYWORDS: Area, Constant Inputs, Garbage Inputs, Garbage Outputs, Gate Count and Power

INTRODUCTION

Power dissipation is an important factor in VLSI design as modern logic circuits offer a great deal of computing power in a small footprint. The combinational logic circuits dissipate heat of KTln2 joules [1] for every bit of information erased during computation, where k = 1.3806505x10-23J/K is Boltzmann constant and T is the operating temperature in degrees at which the computation is carried out. Also, as Moore predicted that the number of transistors approximately doubles in every eighteen months and if this trend continues to hold, in the near future more and more energy will be lost due to the loss of information. Charles Bennett [2] showed that energy loss could be avoided or even eliminated if the computations are carried out in reversible logic and also proved that circuit built from reversible gates have zero power dissipation. Thus reversible logic appears to be promising in future low power design applications.

Reversible circuits are similar to conventional logic circuits except that they are built from reversible logic gates. In reversible gates, there is unique i.e., one-to-one mapping between the inputs and outputs, which is not the case in conventional logic. Reversible gates are used in quantum computing system as quantum operations are reversible in nature. The reversible circuit/gate has the following characteristics: (i) has equal number of inputs and outputs (ii) the gate output, which is not used as primary output in the circuit is called garbage output (iii) the input which is used as control input to the gates is called constant/garbage input (iv) the fan-out of each gate is equal to one. A copying circuit is used if two copies of a signal are required and (v) the resulting circuit is acyclic

An efficient design in reversible logic should have the following features [3]: (a) use minimum number of reversible logic gates (b) should have less number of garbage outputs (c) less number of constant inputs and (d) minimization of quantum cost. Addition and multiplication operations are widely used arithmetic operations in many computations. High speed multiplier circuits are of particular interest in processor design.

Contribution: In this paper, we presented a reversible 4x4 multiplier with the design of new reversible gate called ABC Gate and GPS Gate. The proposed multiplier circuit is efficient compared to the existing designs in terms of gate counts, garbage outputs, constant inputs area and power and this design can be generalized to construct reversible nxn multiplier

Organization: The paper is organized into the following sections. Section 2 is an overview of basic reversible gates. The background work is described in section 3. Section 4 is about new reversible gate and the proposed multiplier design, results and discussions of the proposed design is presented in section 5 and conclusions are contained in section 6.

BASIC REVERSIBLE GATES

Reversible logic gates are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. A reversible circuit can be realized by using reversible gates only. The simplest reversible gate is NOT gate and is a 1*1 gate.

NOT GATE

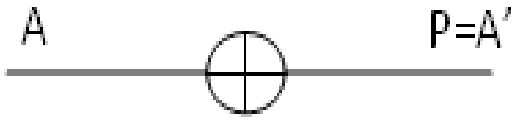

Figure 1: NOT Gate

FEYNMAN GATE

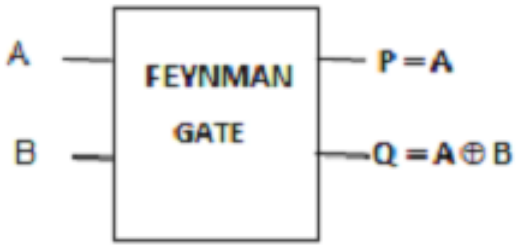

Figure 2: Feynman Gate

FREDKIN GATE

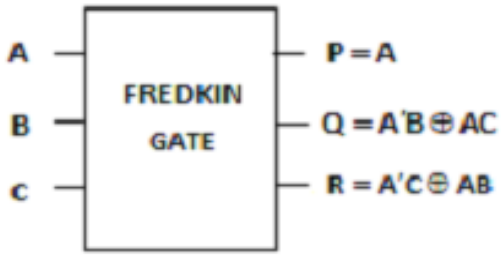

Figure 3: Fred Kin Gate

TOFFOLI GATE

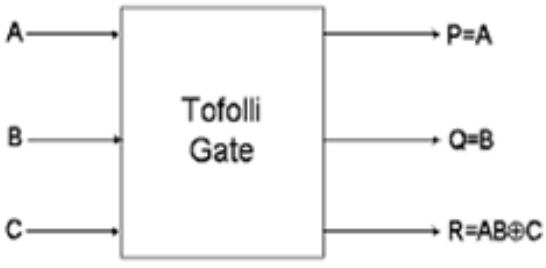

Figure 4: Toffoli Gate

PEERS GATE

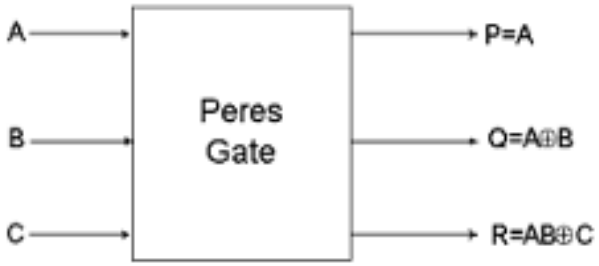

Figure 5: Peres Gate

DOUBLE FEYNMAN GATE

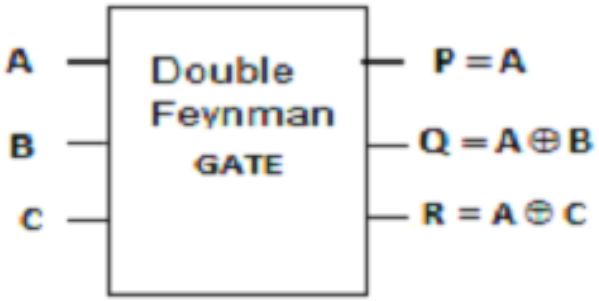

Figure 6: Double Feynman Gate

TSG GATE

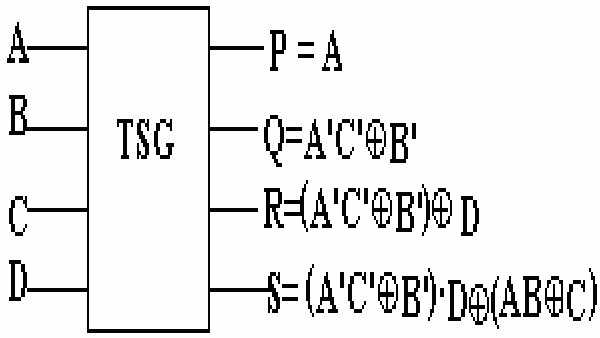

Figure 7: TSG Gate

PROPOSED ABC Gate

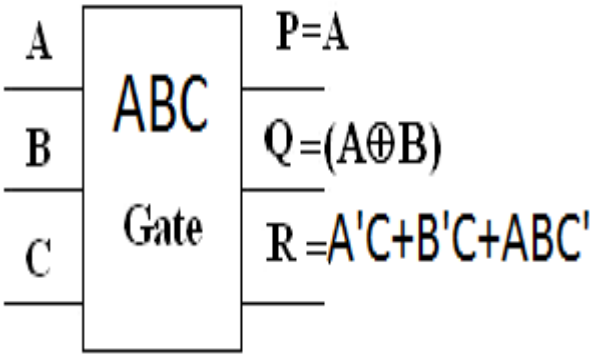

Figure 8: Proposed 3×3 Reversible ABC Gate

Table 1: Truth Table for ABC Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

PROPOSED GPS Gate

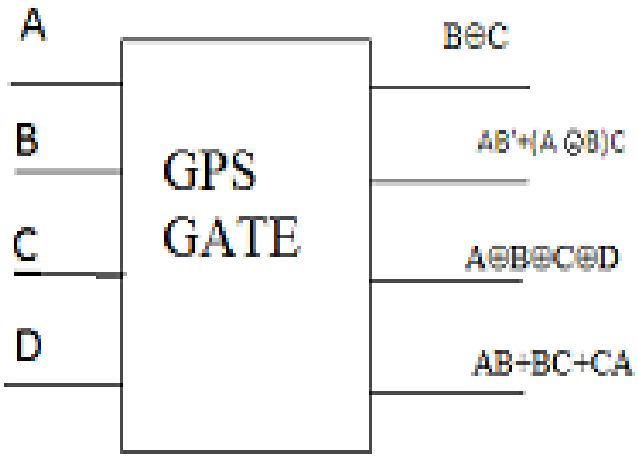

Figure 9: Proposed 3×3 Reversible GPS Gate

Table 2: Truth Table for GPS Gate

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	0
0	1	0	0	1	0	1	0
0	1	0	1	1	0	0	0
0	1	1	0	0	0	0	1
0	1	1	1	0	0	1	1
1	0	0	0	0	1	1	0
1	0	0	1	0	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	1
1	1	1	0	0	1	1	1
1	1	1	1	0	1	0	1

To construct reversible gates with minimum number of transistor count, design of two input XOR gate, OR gate and AND gate are discussed which have minimum number of transistor count.

TRANSISTOR IMPLEMENTATION OF LOGIC GATE USING GDI METHOD

GDI Basic Cell

The GDI method [1] is based on the use of a simple cell as shown in Figure 10. At a first glance the basic cell resembles the standard CMOS inverter, but there are some important differences, GDI cell contains three inputs – G (the common gate input of the nMOS and Pmos transistors), P (input to the outer diffusion node of the pMOS transistor) and N (input to the outer diffusion node of the nMOS transistor). The Out node (the common diffusion of both transistors) may be used as input or output port, depending on the circuit structure.

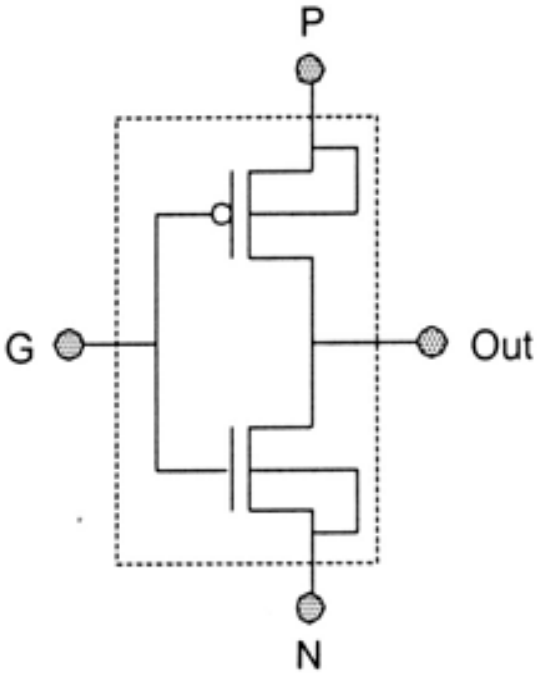

Figure 10: GDI Basic Cell

Table 3 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions require a complex (6-12 transistors) gate in CMOS (as well as in standard PTL implementations), but are very simple (only two transistors per function) in the GDI design methodology. GDI enables simpler gates, lower transistor count, and lower power dissipation.

Table 3: Some Logic Functions that Can be Implemented Using Single GDI Cell

N	P	G	OUT	FUNCTION
B	1	A	A'+B	F1
0	B	A	A'B	F2
B	0	A	AB	AND
1	B	A	A+B	OR
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

Design of XOR Gate

The design of XOR gate is shown in Figure 11. The design is based on GDI method. Here two GDI cells are considered in which one cell in taken as basic inverter and for the second cell A input given to P, B input is given to G and output of first cell is given to N.

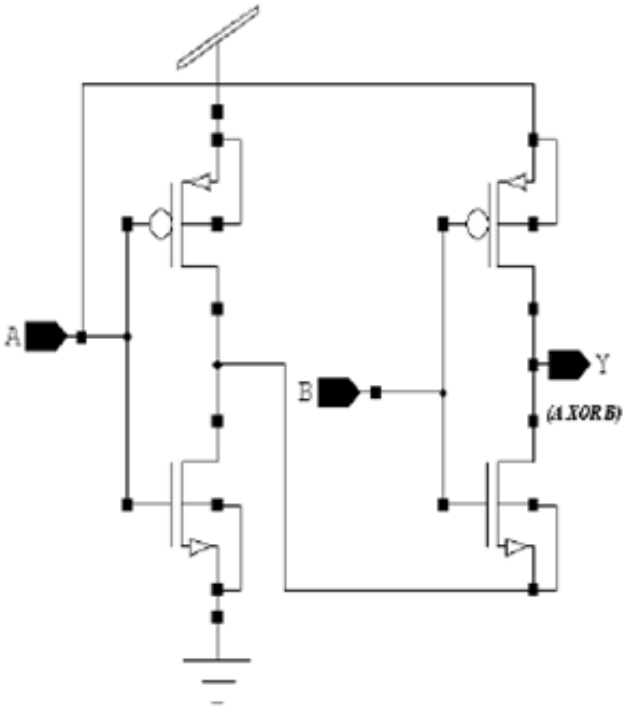

Figure 11: XOR Gate Using GDI

Design of OR gate

The design of OR gate is shown in Figure 12. To make the basic GDI cell to work as OR gate input B is given to P,input A is given to G, and VDD is given to N.

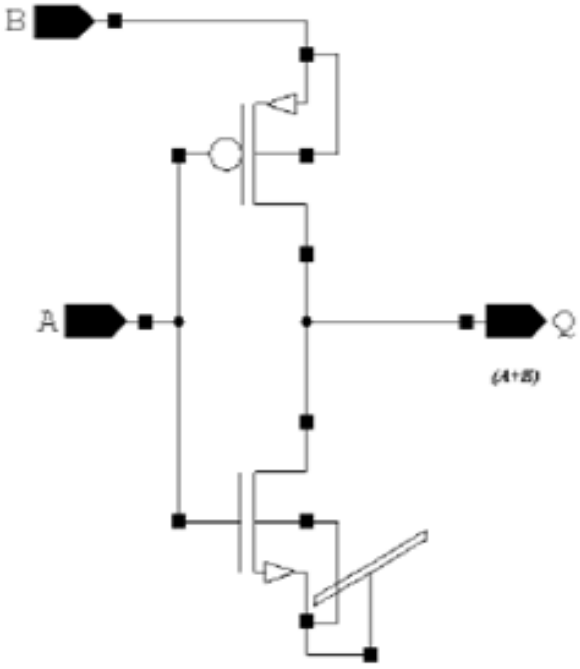

Figure 12: OR Gate Using GDI

Transistor Implementation of Proposed Reversible Gates

In this paper two new reversible gates are proposed. The main intension is to implement the reversible Multiplier with minimal number of reversible gates, transistor count, and garbage bits.

Proposed Reversible ABC Gate

The ABC gate takes A, B, C as inputs and Produce P, Q, R as outputs and corresponding functionalities shown in Figure 8. The transistor implementation of ABC gate using GDI is shown in Figure 13.

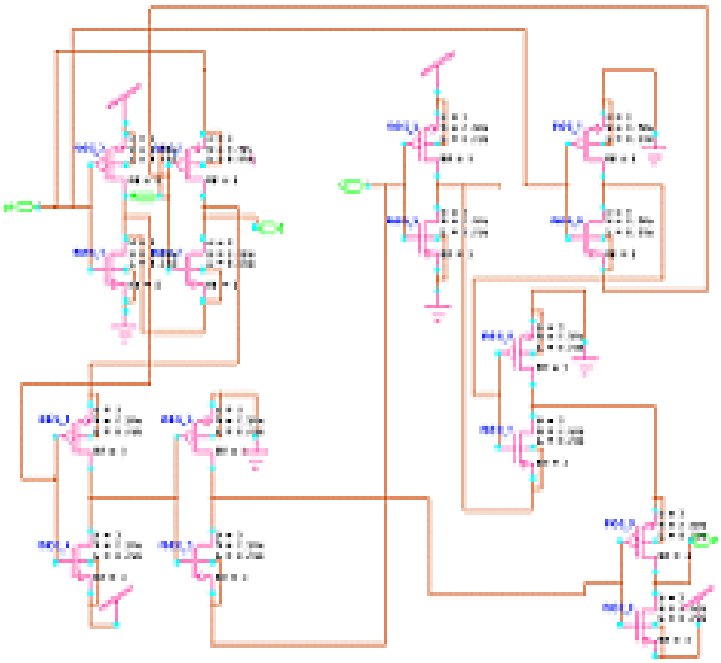

Figure 13: Transistor Implementation of Proposed ABC Gate

Proposed Reversible GPS Gate

The GPS gate takes A, B, C as inputs and Produce P, Q, R as outputs and corresponding functionalities shown in Figure 9. The transistor implementation of GPS gate using GDI is shown in Figure 14

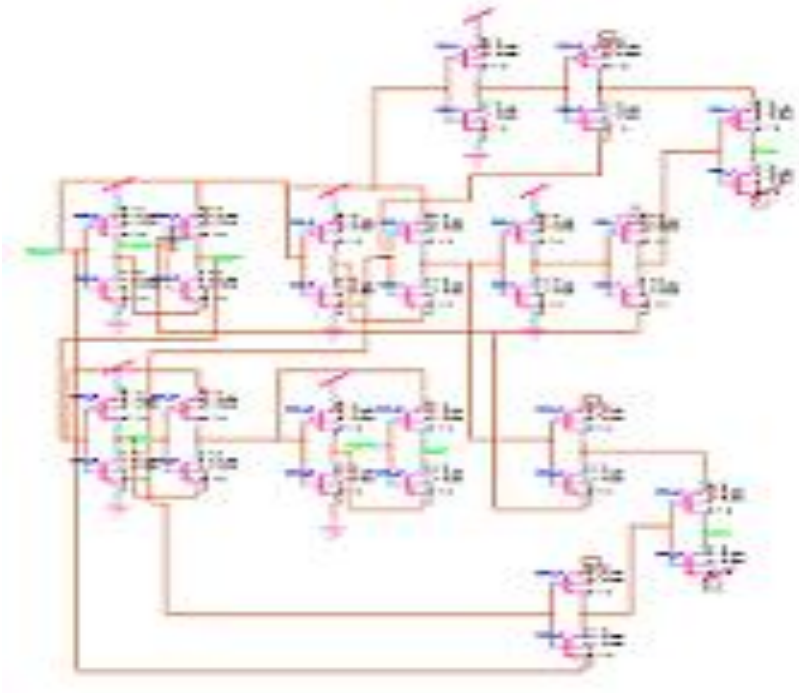

Figure 14: Transistor Implementation of Proposed GPS Gate

PROPOSED MULTIPLIER DESIGN

Reversible Multiplier Design

In this paper the multiplier designed in GDI low power technique is compared with the standard conventional cmos. A 4×4 Reversible multiplier has two parts..One is Partial Product term Generation (PPG) and other one is multi operand Addition circuit (MOA).The details of these two parts are following sections.

Partial Product Term Generation

The basic operation of 4×4 multiplier as shown in figure 15. It consist of sixteen partial products of the form Xi .Yi , where I vary between 0 and 3.

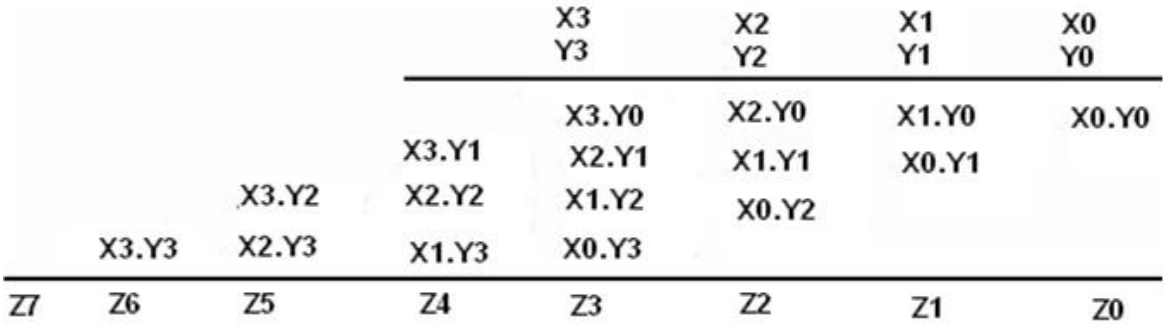

Figure 15: The Basic Operation of a 4×4Multiplier

PPG circuit using Toffoli gate is as shown in figure 16. Here 16 Toffoli gates are used to generate sixteen Partial products as shown in figure 15.

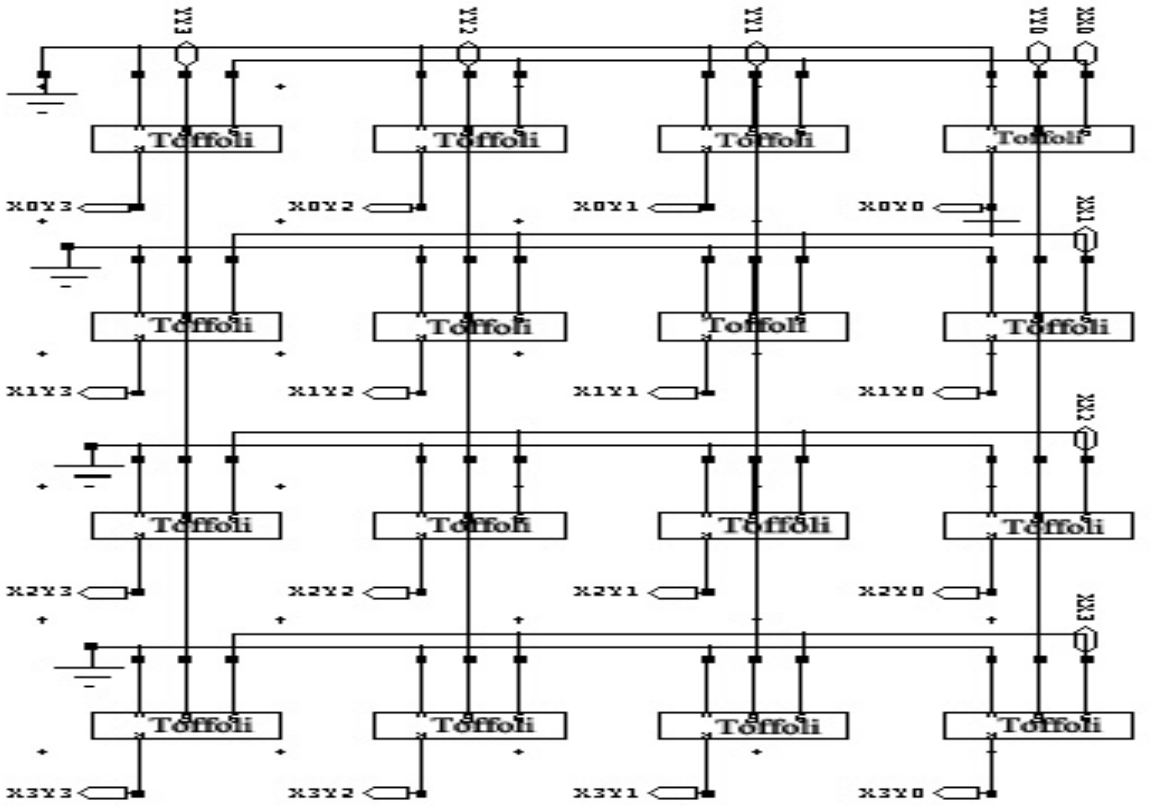

Figure 16: Proposed Partial Products Generation Circuit Using Toffoli Gate

Multi Operand Addition Circuit

The addition of partial products using new proposed gates called ABC and GPS gates is as shown in figure 17.The basic cell for such a multiplier is full adder using GPS gate with here inputs and one constant input, two garbage outputs and half adder using ABC gate with two inputs and one constant output, one garbage output. The proposed multiplier uses eight GPS gates and four ABC gates, Sixteen Tofolli gates for partial product terms generation.

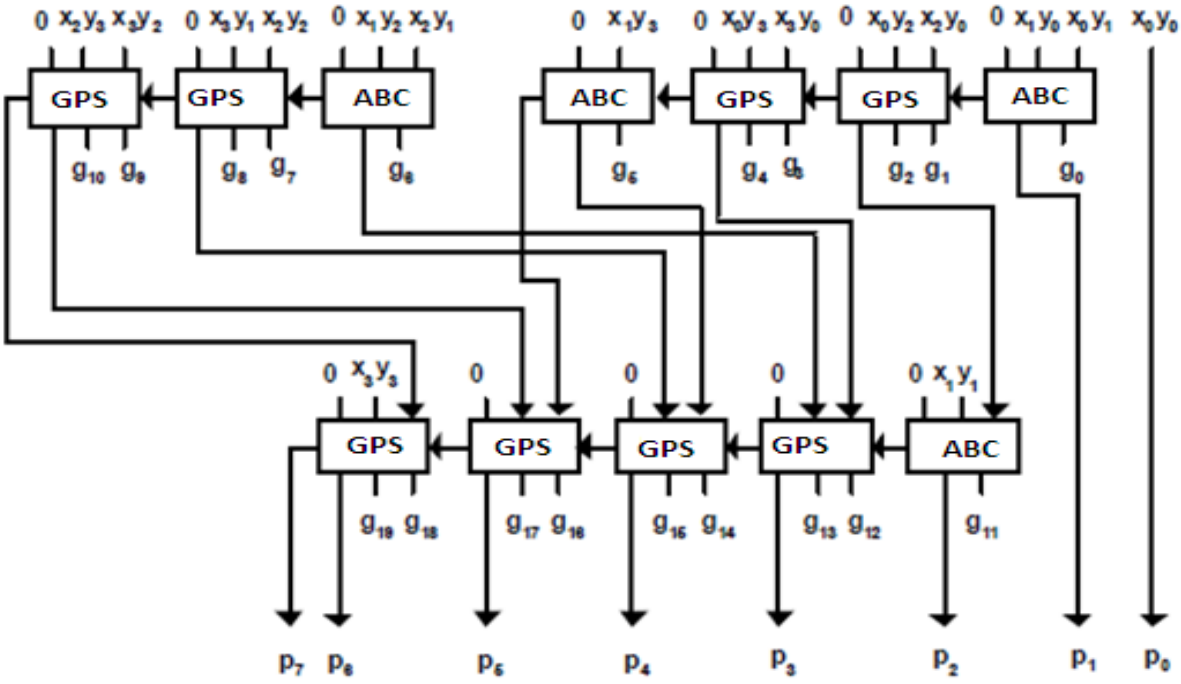

Figure 17: 4×4 Multi Operand Addition Circuit Using Proposed Gates

RESULTS AND DISSCUSIONS

The proposed Reversible multiplier using ABC and GPS gates are realized using tanner tools to simulate the output. The output waveform is depicted in Figure 18.

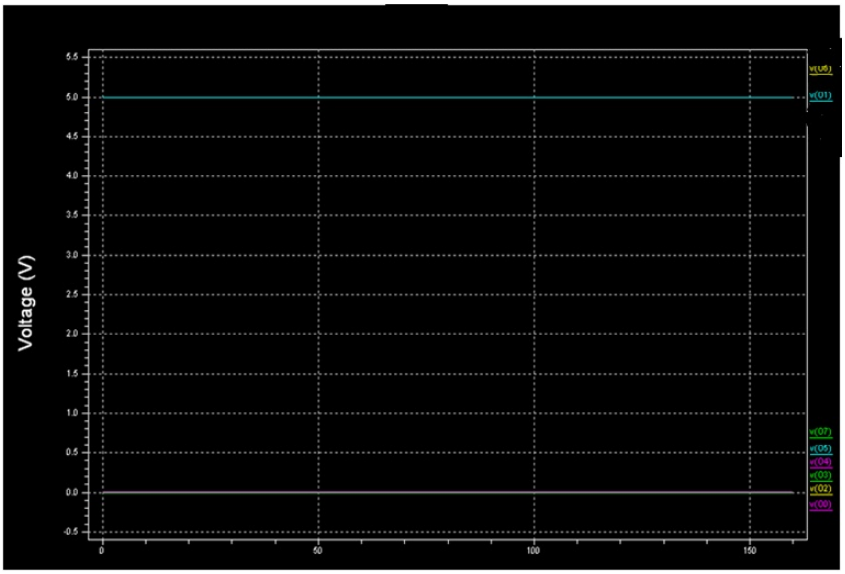

Figure 18: Output Waveform of Reversible Multiplier

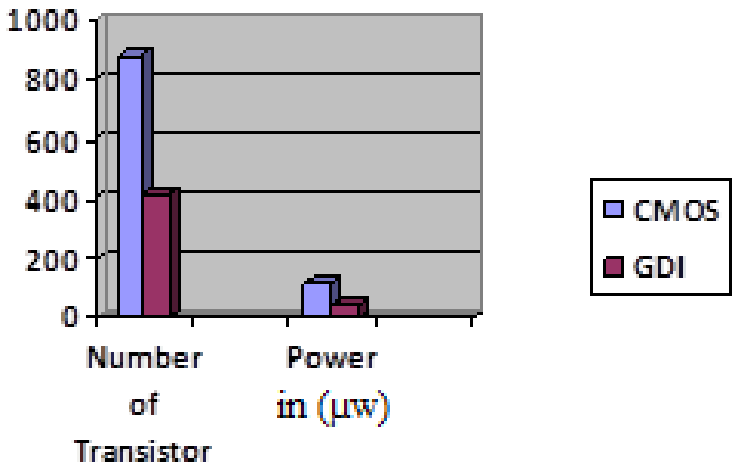

Figure 19: Comparision of Proposed Multiplier with CMOS and GDI Techniques

Gate Count/Hardware Complexity: one of the major factors of a circuit is measured in terms of number of gates. It can be proved that the proposed circuit is better than the existing approaches in terms of hardware complexity. In [10], the total number of reversible gates required is 40, [11] requires 42 and in [12] total number of gates required is 44. The proposed reversible multiplier design requires 12 gates.

Garbage Inputs: Number of constant inputs is one of the main factors in designing a reversible logic circuit. The input used as a control input by connecting to logical low or logical high to get the required function at the output is called garbage/constant input. The proposed reversible multiplier circuit requires 16 constant inputs, but the design in [10], [11] and [12] requires 52, 42 and 44 respectively. So, it is clear that our design approach is better than existing designs in terms of constant inputs.

Garbage Outputs: the output of the reversible gate that is not used as a primary input or as input to the other gates is referred as garbage output. Optimizing garbage outputs is one of the other main constraints in designing reversible logic circuit. The proposed reversible multiplier circuit produces 23 garbage outputs, but the design [10], [11] and [12] produces 52, 49 and 52 garbage outputs respectively. Therefore, it is clear that design is better that the existing counterparts in terms of number of garbage outputs. From the above discussion, it is evident that the proposed reversible multiplier circuit is better than the existing designs in terms of gate counts, quantum cost, garbage inputs and garbage outputs.

Table 4: Comparision of Proposed and Existing Reversible Multiplier

	Gate Count	Garbage Inputs	Garbage Outputs
[10]	42	42	49
[11]	44	44	52
[12]	32	40	40
Proposed	28	16	23

Table 5: Comparision of Proposed Multiplier with the CMOS and GDI Techniques

Proposed Multiplier	Number of Transistors	Power in (µw)
CMOS	880	115
GDI	416	43

CONCLUSIONS

In this paper, design of the 4*4 reversible multiplier circuit with new reversible ABC and GPS Gate is presented.It is seen that the power and area of the GDI technique are reduced with that of that standard conventional cmos technique. And the number of gates, garbage inputs, garbage outputs are less in proposed design compared to the existing approach. The design is very useful for the future computing techniques like ultra low power digital circuits and quantum computers.

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